WHAT IS CLAIMED IS:

1. A method of soft bit computation for a reduced-state equalizer, comprising the steps of:

(a) computing a first set of soft bits for bits transmitted in a received signal, wherein the first set is computed using a reduced-state trellis with finite non-zero delay

(b) calculating hard decisions in response to the received signal, and

(c) ensuring that substantially all soft bits are computed, by employing zero-delay soft decision-making or decision-feedback equalization to compute a second set of soft bits, while also using the hard decisions to compute the second set.

2. The method of claim 1, wherein the soft bits are log-likelihood ratios.

3. The method of claim 1, wherein the finite non-zero delay is K-1, wherein K represents a truncated impulse response length, wherein K=0 for the zero-delay soft decision-making, and wherein K is less than a non-truncated impulse response length L unless K is equal to L.

4. The method of claim 1, wherein the method includes recursion to compute the first set, and the recursion includes only forward recursion which is sufficient recursion.

5. The method of claim 1,

wherein the steps are performed in a sequence (a), (b), and (c) one after another,

wherein step (c) is performed so that the first set of soft bits and the second set of soft bits are soft bits for two different sets of bits, and

wherein the hard decisions are calculated using the first set of soft bits.

6. The method of claim 1, wherein step (c) is performed before step (a), and wherein a soft bit computed in step (c) for a certain bit is replaced with a soft bit computed in step (a) if a soft bit for the certain bit is computed in step (a).

7. The method of claim 1, wherein step (a) is performed for as many bits as possible while maintaining acceptable implementation complexity.

8. The method of claim 1, wherein the trellis has a number of states S and a number of taps K, and wherein 2S equals 2 to the K power, i.e. $2S=2^K$.

9. The method of claim 1, wherein the computation of step (a) produces soft bits using a maximum a posteriori technique.

10. The method of claim 9, wherein the maximum a posteriori technique is a max-log maximum a posteriori technique.

11. The method of claim 1, wherein the computation of step (a) produces soft bits with reduced state sequence estimation.

12. The method of claim 1, wherein the computation of step (a) utilizes a maximum likelihood technique.

13. The method of claim 1, wherein the computation of step (a) produces soft bits with decision feedback partial sequence equalization.

14. The method of claim 6, wherein the second set of soft bits are computed in step (c) using the decision-feedback equalization which provides information as to a reduced number of states that will be needed for the computation in step (a).

15. The method of claim 14, wherein the computation in step (a) employs decision feedback partial sequence equalization.

16. The method of claim 1, wherein the hard decisions are used to compute soft bits so as to reduce error propagation.

17. The method of claim 1, wherein the zero-delay soft decision-making is performed using a trellis.

18. The method of claim 1, wherein the decision-making of step (c) is implemented with a maximum complexity that is twice as complex as implementation of decision-feedback equalization would be.

19. The method of claim 18, wherein the zero-delay soft decision-making of step (c) is performed according to a rule described mathematically as follows:

$$\beta_{0delay}(s_{k+1} = a_k) \approx \min_{(s_k)}\{\mu(s_k) + \lambda(s_k, s_{k+1})\}$$

in which beta represents a zero-delay log symbol probability function, s_k denotes a previous symbol decision, s_{k+1} denotes a current symbol decision, a_k represents a symbol of a modulation alphabet, min is a minimizing function, and mu (μ) and lambda (λ) represent two paths connecting two states.

20. The method of claim 1, also comprising the steps of:

(d) generating further hard decisions using a traceback operation,

(e) checking if the further hard decisions generated using the traceback operation match the hard decisions already generated using the trellis,

(f) replacing soft bits generated using the trellis with the further hard decisions generated using the traceback operation, if the further hard decisions generated from the traceback operation fail to match respective hard decisions already generated using the trellis.

21. The method of claim 1, wherein the computation of step (a) employs a Viterbi algorithm.

22. The method of claim 21, wherein the computation of step (a) employs a soft output Viterbi algorithm.

23. The method of claim 1, wherein the zero-delay computation of step (c) includes the steps of:

establishing a first subset of signals and a second subset of signals by Euclidean partitioning which reduces trellis size to two states corresponding to the first subset and the second subset respectively,

determining which of the two states is a more likely state,

computing Euclidean distances for at least all paths corresponding to the more likely state, and

using only the paths corresponding to the more likely state to perform the computation of step (c).

24. The method of claim 10, wherein the hard decisions are computed using the max-log maximum a posteriori technique.

25. The method of claim 11, wherein the hard decisions are computed in step (b) using the reduced state sequence estimation or decision feedback partial sequence estimation.

26. The method of claim 24, wherein the decision feedback equalization is employed in step (c) according to a rule described mathematically as follows:

$$\beta_{DFE}(a_k) \approx \| \; r_k - (a_k h_o + \sum_{j=1}^{L-1} b_{k-j} h_j) \; \|^2$$

in which beta represents a log symbol probability function, a_k represents a symbol of a modulation alphabet, r_k is a received signal, b_k are the hard decisions, and h_k is channel impulse response length.

27. The method of claim 25, wherein the decision feedback equalization is employed in step (c) according to a rule described mathematically as follows:

$$\beta_{DFE}(a_k) \approx \| \; r_k - (a_k h_o + \sum_{j=1}^{L-1} b_{k-j} h_j) \; \|^2$$

in which beta represents a log symbol probability function, a_k represents a symbol of a modulation alphabet, r_k is a received signal, b_k are the hard decisions, and h_k is channel impulse response length.

28. A reduced-state equalizer (200) capable of providing soft bits to a decoder (290) in order to enhance reliability of channel decoding subsequent to equalization, the reduced-state equalizer comprising:

a reduced-state trellis module (220), responsive to a received bit signal (260), for providing a first soft bit signal (280) and a hard decision signal (270); and

a gap-filler module (210), responsive to the received bit signal and also responsive to the hard decision signal (270), for providing a second soft bit signal (292),

wherein the second soft bit signal (292) includes soft bits that are absent from the first soft bit signal, so that the first and the second soft bit signals include soft bits for substantially all bits in the received bit signal (260),

wherein the reduced-state trellis module (220) is configured to operate with finite non-zero delay, and

wherein the gap-filler module (210) is configured as a decision feedback equalizer or as a zero-delay soft decision-maker.

29. A receiver for a wireless communication device, configured to mitigate intersymbol interference contained in a received signal (260), comprising:

a decoder (290), responsive to a first soft bit signal (280) and a second soft bit signal (292), for providing a reliably decoded signal (297),

a reduced-state equalizer (200) capable of providing soft bits to the decoder (290) in order to enhance reliability of channel decoding subsequent to equalization, the reduced-state equalizer including

a reduced-state trellis module (220), responsive to a received bit signal (260), for providing the first soft bit signal (280) and a hard decision signal (270); and

a gap-filler module (210), responsive to the received bit signal and also responsive to the hard decision signal (270), for providing the second soft bit signal (292),

wherein the second soft bit signal (292) includes soft bits that are absent from the first soft bit signal, so that the first and the second soft bit signals include soft bits for substantially all bits in the received bit signal (260),

wherein the reduced-state trellis module (220) is configured to operate with finite non-zero delay, and

wherein the gap-filler module (210) is configured as a decision feedback equalizer or as a zero-delay soft decision-maker.